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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: February 5, 2002 (use as many sheets as necessary)				Complete if Known	
				Application Number	Unassigned
				Filing Date	02/05/2002
				First Named Inventor	Igor KOUZNETSOV et al.
				Group Art Unit	Unassigned
				Examiner Name	Unassigned
				Attorney Docket Number	035905-0118
Sheet	1	of	7		

10/066376
 02/05/02

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
LP	A1	5,427,979		Chang	06/27/1995	
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Examiner Signature	LONG PHAM	Date Considered	3/20/04
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		U.S. Patent Document			
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LP	A69	JOHN H. DOUGLAS: "The Route to 3-D Chips," High Technology, September 1983, pgs. 55-59, Vol. 3, No. 9, High Technology Publishing Corporation, Boston, MA		
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LP	A71	O. BELLEZZA et al.: "A New Self-Aligned Field Oxide Cell for Multimegabit Eproms," IEDM, pgs. 579-582, IEEE	
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	A117	KUNIYOSHI YOSHIKAWA et al.: "An Asymmetrical Lightly Doped Source Cell for Virtual Ground High-Density EPROM's," IEEE Transactions on Electron Devices, pgs. 1046-1051, Vol. 37, No. 4, April 1990, IEEE		
	A118	VIVEK SUBRAMANIAN: "Control of Nucleation and Grain Growth in Solid-Phase Crystallized Silicon for High-Performance Thin Film Transistors," A Dissertation Submitted to the Department of Electrical Engineering and the Committee of Graduate Studies of Stanford University in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy, June 1998		
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	A121	DIETMAR GOGL et al.: "A 1-Kbit EEPROM in SIMOX Technology for High-Temperature Applications up to 250° C," IEEE Journal of Solid-State Circuits, October 2000, Vol. 35, No. 10, IEEE		
	A122	STANLEY WOLF: "Silicon Processing for the VLSI Era," Semiconductor Memory Process Integration, Volume 2		

Examiner Signature	Long Pham	Date Considered	3/20/04
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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: February 5, 2002 (use as many sheets as necessary)				Complete if Known	
				Application Number	Unassigned
				Filing Date	02/05/2002
				First Name of Inventor	Igor KOUZNETSOV et al.
				Group Art Unit	Unassigned
				Examiner Name	Unassigned
				Attorney Docket Number	035905-0118
Sheet	7	of	7		

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM- DD-YYYY	Pages, Column, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
LP	A123	5,383,149		Hong	01/17/1995	
	A124	5,572,046		Takemura	11/05/1996	
OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.				T ⁶
LP	A125	WEB PAGE-ime.org.sg; "Tachyon and IME to Build 3D Chips for Greater Speed and Performance," Press Release, dated January 18, 2002				
LP	A126	ICHIRO FUJIWARA et al.: "MONOS Memory Cell Scalable to 0.1µm and Beyond," pages 117-118				

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